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|---|---|
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| **ART UNIT** | **PAPER NUMBER** |
| 2654 | |

DATE MAILED: 09/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/737,553 | KEMPE, ANDRE | |
| | **Examiner** | **Art Unit** | |
| | Thomas E Shortledge | 2654 | |

***-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --***

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) _1-18_ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1-18_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _04/04/2001_.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

## DETAILED ACTION

### *Drawings*

1. Figures 1-12 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: All of Figures 17,18, 21, 23, 24, 44, 49, 51, 65, 69, 70,71 and Fig. 19, elements 1118,1120,1122,1124,1126,1128,1130, Fig. 36, 2000,2001,2002,2005,2004, Fig. 43, 2202,2203,2206,2209,2210,2208,2211, Fig. 47, elements 2604,2605,2608,2609,2611,2612, Fig. 54, elements 3300,3306, Fig. 56, elements, 3500,3502,3501,3504,3503, and Fig. 59, elements, 3728,3730,3732,3734,3736,3738. Correct drawing sheets in compliance with 37

CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

## *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chung et al. (6,278,973) in view of Mohri et al. (6,574,597), an in further view of Devadas et al. (Decomposition and Factorization of Sequential Finite State Machines)

As to claims 1 and 14, Chung et al. teach:

assigning to each state a set of epsilon loops and a unique diacritic representative of the set; each epsilon loop in the set of epsilon loops beginning and ending at a corresponding state; said assigning step defining a first representative of the input FST and a second representative of the input FST

(representing arcs within the transducers with the symbol "epsilon" which denotes a "free move" or empty set, fig. 9 contains a finite-state transducer with states 0-2, in which each state contains an epsilon loop, beginning and ending at that state; two transducers T1 and T2 that are combinable. Therefore, T1 and T2 would be divisions of the resulting transducer, col. 8, lines 33-39, Fig. 9, and col. 8, lines 59-63 (respectively)).

building a factor by inserting into the first representation of the input FST an auxiliary state for each state with a non-empty set of epsilon loops; wherein each auxiliary state has an arc that leads from the auxiliary state to the corresponding state and emits the corresponding unique diacritic when traversed, (creating a new state machine N from input machine M, in which a filter can be used to introduce an epsilon symbol that represents an arc in the state machine, when traversed the symbol will be produced, col. 8, lines 19-45);

removing from the first factor at least one epsilon loop without removing the arcs corresponding to the epsilon loop (each path with in the factor from the input to the output corresponds to a distinct way of using epsilon-transitions. Retaining only one of these paths while removing the others, col. 9, lines 3-7. It would be inherent to see that when the epsilon loops are removed, the arcs corresponding to the epsilon loop are kept intact since the factor is able to still travel between states)

removing from the second factor all paths having partial epsilon loops, (each path with in the factor from the input to the output corresponds to a distinct way of using epsilon-transitions (col. 9, lines 3-7). All redundant paths are

removed, including paths that have partial epsilon loops, only allowing one path to be traveled between the two states).

mapping each diacritic in the second factor to a corresponding set of epsilon loops (epsilon-transitions are distinguished by different indices, col. 8, lines 60-61).

Chung et al. do not teach:

building a first factor

building a second factor by inserting into the second representation of the input FST two auxiliary arcs for each state with a non-empty set of epsilon loop; wherein the two auxiliary arcs are labeled with a diacritic, and wherein a first of the auxiliary arcs leads from an initial state to its corresponding sate, and a second of the auxiliary arcs leads from its corresponding state to a final state.

However, Mohri et al. teach disambiguating a model by labeling alternatives with auxiliary arcs or symbols, and figure 2a depicts a factor that has its first and second state connected by a single arc, and another state connected to a final state by a single arc (col. 7, lines 60-65, and figure 2a).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to combine epsilon-assigning technique of Chung et al. with the auxiliary arc substitution of Mohri et al. for improving the efficiency of speech recognizer using large vocabulary applications as taught by Mohri et al. (col. 2, lines 27-29).

Chung et al. and Mohri et al. do not teach building a first and second factor.

However Devadas et al. do teach using a procedure to find all exact factors in a machine, (page 1211, col. 1)

Therefore it would have been obvious to one of ordinary skill at the time of the invention to combine the epsilon-assigning technique of Chung et al. with the auxiliary arc substitution of Mohri et al. and with the factoring methods of Davades et al. for increased performance as taught by Davades et al. (col. 1, page 1206).

As to claim 2, Chung et al. teach minimizing the factors (using a filter to further refine the finite-state machines, col. 8, lines 32-33).

Chung et al. and Mohri et al. do not teach of a first and second factor.

However Devadas et al. do teach using methods of decomposition on a finite-state machine to create two submachines, M1 and M2.

Therefore it would have been obvious to one of ordinary skill at the time of the invention to combine the minimizing of factors with the auxiliary arc substitution of Mohri et al. and with the decomposition methods of Davades et al. for increased performance as taught by Davades et al. (col. 1, page 1206).

As to claim 3, Chung et al. do not teach concatenating at least one boundary symbol to the input FST; and minimizing the input FST.

However, Mohri et al. teach using the “$” as an end-of-utterance symbol used to make the result sequential, (col. 7, lines 47-48).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to combine epsilon-assigning technique of Chung et al. with the boundary symbol of Mohri et al. for improving the efficiency of speech recognizer using large vocabulary applications as taught by Mohri et al. (col. 2, lines 27-29).

As to claim 4, Chung et al teach:

temporarily replace each arc of the epsilon loop with a diacritic to define a sequence of diacritics, (an arc with an a sequence arcs can be represented by a symbol, creating a sequence of those symbols, col. 6, lines 39-41).

formulate a constraint that disallows the sequence of diacritics (a filter that is able to remove epsilon-transitions, col. 9, lines 9-13).

compose the constraint with the first factor (the filter applied to a transducer, col. 9, lines 9-12).

replace any remaining diacritics with an epsilon symbol, (an empty word or free move can be represented by an epsilon, col. 8, lines 38).

As to claim 5, Chung et al. teach the step of removing all paths having partial epsilon loops from the second factor further comprises the step of mapping any sequence of two identical diacritics to itself and inserting a corresponding epsilon loop there between, (comparing states and removing redundant epsilon-transitions which can be represented by a symbol, reducing

the overall number of paths and inserting one of the redundant epsilon-transitions into the transducer (col. 9, lines 9-13).

As to claim 6, Chung et al. teach partial epsilon loops are paths with an input side having one of the unique diacritics only once, (figure 10, shows a FST that contains an epsilon loop, containing only one of the symbols representing these arcs, Fig. 10 arc from state 2.2 to 3.2)

As to claim 7, Chung et al teach the said step of removing from the second factor all paths having epsilon loops further comprises removing arcs fro the second factor (removing all redundant epsilon paths along with their arcs, col. 9, lines 3-7).

As to claim 8, Chung et al. teach the step of removing from the second factor all paths having epsilon loops further comprises rearranging arcs in the second factor (a filter can be used to remove redundancy of the epsilon-transitions (col. 9, lines 9-12). It would be obvious that once paths are removed, the remaining paths would be rearranged to maintain order within the FST).

As to claim 9, Chung et al. teach a selected state has a non-empty set of epsilon loops if starting at the selected state a sequence of arcs, each having an epsilon label, is traversed in the input FST that terminates at the selected state, (within the transducers T1 it is taught that if there is an epsilon-transition, it would

be possible to move to state 1, then once a match is found it would lead to state 0, where it is terminated (col. 9, lines 21-24). It is obvious that such a process can be described as starting at a selected state, traversing through a FST and then terminated at this selected state. Therefore this would lead to a selected state having a non-empty set of epsilon loops.)

As to claims 10 and 15, Chung et al. and Mohri et al. do not teach factoring the first factor into a functional FST and a Fail-Safe FST

However, Devadas et al. teach of dividing a finite-state machine into two sequential finite-state machines, in which one of the sub-machines retains the behavior of the original machine, col. 2, page 1206. These sub-machines perform the same operations as the original machine, therefore, they are able to have the same characteristics in that one sub-machine can be unambiguous while the other can be ambiguous (fail-safe).

Therefore it would have been obvious to one of ordinary skill at the time of the invention to combine the epsilon-assigning technique of Chung et al. with the auxiliary arc substitution of Mohri et al. and with the sub-machines of Davades et al. for increased performance as taught by Davades et al. (col. 1, page 1206).

As to claims 11 and 16, Chung et al. teach the functional FST, fail safe FST, and the second factor are adapted for performing language processing (the transducers can be used in language processing, col. 6, lines 10-11).

As to claim 12 and 17, Chung et al. teach the language processing comprises one of tokenization, phonological analysis, morphological analysis, disambiguation, spelling correction and shallow parsing, (modeling of sound patters includes language model, word pronunciation models, and phone models, col. 1, lines 42-45).

As to claim 13 and 18, Chung et al. teach the functional FST, the fail-safe FST and the second factor form part of a lexical transducer (lexicon models that can constructed by various networks linked together, these networks can be made up of an FST, col. 1, lines 44-46, and col. 2, line 51).

***Conclusion***

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Mohri, (6,032,111), Reed (5,095,432), and Kaplan (5,721,939).

Mohri teaches using finite-state machines to create context dependent rewrite rules.

Reed teaches the use of finite-state machines to perform fast parsing of natural language.

Kaplan teaches the use of finite-state machines to tokenize text.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas E Shortledge whose telephone number is (703)605-1199. The examiner can normally be reached on M-F 8:00 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Talivaldis Smits can be reached on 703-306-3011. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TS
8/27/04

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